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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/627,056	07/25/2003	Daniel J. Smith	003921.00151	2207

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EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 01/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/627,056	SMITH ET AL.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-10,14,15 and 18-26* is/are rejected.

7)☒ Claim(s) *3,11-13,16 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/627,056 filed on 7/25/2003. Claims 1-32 remain pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-2, 4-10, 14-15, 18, 20-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Amparan et al. (US 2004/0245011).

4. As to claims 1 and 27, Amparan et al. teach power plane slitting of a printed circuit board (PCB) (the PCB is a multi-layer PCB) using contour method. The power plane splitting method calculates a potential field of a power plane of a PCB by assigning potential values to components coupled to the PCB (PCB included outline) and solving for potential field values at locations between the components (a power fanout). The potential field is used in defining boundaries (wire frames) between the components by selecting contours of constant potential within the calculated potential field. The boundaries are used to create traces (defining a trace) on the power plane. The traces connect the components so that each component with a same potential

value is coupled to a same power supply (at least see summary, [0017-24]). Fig. 7-8 shown different power plane splitting (Fig. 7) and routing within different boundaries for different associated potential values requirements (Fig. 8). Accordingly, Amparan et al. substantially teach similar claimed limitations.

5. As to claims 2 and 28, Amparan et al. teach an important characteristic of a trace is trace width and the power plane slitting method is used to maximize trace widths of conductor areas without allowing shorting between adjacent traces [0024] and a potential solver is used to compute a potential field at one or more locations between one or more nodes. Amparan et al. teach a user verifies that a trace corresponding to a boundary created has sufficient width and a sufficient resistance to meet design requirements [0033].

6. As to claims 8 and 10, Amparan et al. teach an important characteristic of a trace is trace width, where the trace can be adjusted (enlarged) based on potential level requirement while preventing shorting between adjacent traces [0024-0025]. Thus, this would suggest the claimed limitations.

7. As to claims 4-5 and 29, Amparan et al. teach in Fig. 7, boundaries illustrate two features of a power plane splitting where nodes coupled to a same power supply are within a single boundary and nodes coupled to different power supplies are not coupled together. Fig. 4, shown layout after applying a contour solver for power plane splitting, where nodes are organized to within different regions according to associated assigned potential values. This would suggest if having any crossover between a first voltage wireframe (a first voltage boundary) and a second voltage wireframe (a second voltage

boundary) the method reconfigures at least one voltage wireframe (boundary) to eliminate a crossover.

8. As to claims 6-7, 9, Amparan et al. teach rearranging an ordering of electrical loads in Fig. 4, where the figure shown layout after applying a contour solver for power plane splitting, where nodes are organized to within different regions according to associated assigned potential values. Fig. 8 shown result of such layout and routing according to electrical requirements within boundaries where line segments 810, 820 and 830 are required different potential voltage levels, where the routing of segments associated with the same potential voltage level or average voltage level is within a boundary. It is noted that current levels and potential voltage levels are alternative design requirements.

9. As to claim 14, Amparan et al. teach a contour solver for power plane slitting. Fig. 4, shown layout after applying a contour solver for power plane splitting, where nodes are organized to within different regions according to associated assigned potential values. The contour solver is to define a location of one or more traces corresponding to the one or more boundaries where the one or more traces connect to node, where nodes coupled to a same power supply are within a single boundary and nodes coupled to different power supplies are not coupled together [0022-0023]. This would suggest reconfiguring the split plane wireframe or boundary.

10. As to claim 15 and 30, Amparan et al. teach the contour has a corresponding area.

11. As to claim 18, Amparan et al. teach the contour solver is to define a location of one or more traces corresponding to the one or more boundaries where the one or more traces connect to node, where nodes coupled to a same power supply are within a single boundary and nodes coupled to different power supplies are not coupled together [0022-0023]. This would result in balancing a first area of the first constituent plane and a second area of the second constituent plane.

12. As to claim 20, Amparan et al. teach a power plane splitting method of PCBs or any electronic circuit fabrication technology [0034]. Thus the repeating step must be included within the method in order to complete the power plane splitting of the PCBs or the any electronic circuit fabrication technology.

13. As to claim 21, Amparan et al. teach a power plane splitting method of a PCB by partitioning the layout into boundaries based different potential levels, where within each boundary nodes are connected to receive the same electrical potentials. The electrical ground potentials are inherently included.

14. As to claim 22, Amparan et al. teach a power plane splitting method of PCBs or any electronic circuit fabrication technology [0034]. Since the PCBs or the any electronic circuit fabrication comprises multi-layers, therefore power split planes are resided on a different layer.

15. As to claim 23, Amparan et al. teach the contour solver is to define a location of one or more traces corresponding to the one or more boundaries where the one or more traces connect to node, where nodes coupled to a same power supply are within a single boundary, and nodes coupled to different power supplies are not coupled

together [0022-0023]. This corresponds to eliminating all of the crossovers since nodes coupled to different power supplies are not coupled together.

16. As to claims 24-26, Amparan et al. teach a power plane splitting method/computer readable medium having instructions for performing the method that apply to PCBs or to any electronic circuit fabrication technology. Thus, this would suggest a multi-layer PCB having a split power plane designed accordingly the method.

17. As to claims 31-32, Amparan et al. teach a power plane splitting method/computer readable medium having instructions for performing the method that apply to PCBs or to any electronic circuit fabrication technology [0034-0037]. Since, the computer implemented method is operable on a computer system having storage medium, monitor, keyboard and processor, the claimed limitations are inherently included.

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claim 19 is rejected under 35 U.S.C. 103(a) as being obvious over Amparan et al. (US 2004/0245011) in view of Das et al., "Channel Routing in Manhattan-Diagonal Model," IEEE, 1995, pp. 43-4.

20. As to claim 19, Amparan et al. teach routing using vertical and horizontal connection, but do not teach diagonal routing with 45-degree connection. Das et al. teach routing with vertical, horizontal and diagonal with 45-degree connections in order to provide more flexibility and minimize routing area (pages 43-44). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have selected connection from the group consisting of a horizontal, vertical, a 45-degree connections in order to provide more flexibility and minimize routing area.

Allowable Subject Matter

21. Claims 3, 11-13, and 16-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art does not teach or fairly suggest adding if a signal via is situated on a first segment, relocating the signal via and moving as recited in the claims.

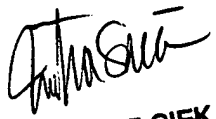
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906. The examiner can normally be reached on Increase Flextime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek



VUTHE SIEK
PRIMARY EXAMINER